

# Effects of texture additive in large-area diamond wire cut multicrystalline silicon solar cells

S. Saravanan, Ch.S.R. Suresh, V.V. Subraveti, K.C. Kumar & U.K. Jayaram, RenewSys India Pvt Ltd, Hyderabad, India

## Abstract

The silicon PV industry has predominantly used silicon wafers sliced by a steel wire, with silicon carbide particles (slurry wire – SW) as an abrasive and polyethylene glycol as a coolant. Low yield, high total thickness variation (TTV), significant material waste and short wire lifetime (and thus high downtime) of SW cutting technology have prompted the wafer slicing industry to develop an alternative technology. Researchers have developed diamond wire (DW) cutting technology for slicing the silicon and demonstrated that it overcomes the drawbacks of SW cutting technology. Although the DW cutting technology has been demonstrated for slicing wafers, the wafer surface is different after the conventional acidic texturing in a silicon solar cell process. It is therefore important to improve the existing process or to develop a new process, in order to produce a homogeneous texturization on DW-cut wafers. In this work, a systematic approach has been pursued to improve the existing process by using an additional etchant (a texture additive) in the acidic mixture. Different etch depths and the corresponding mean reflectance were studied. Optical and morphological studies on DW-cut wafers processed with and without a texture additive have been carried out and interpreted in terms of electrical performance.

## Introduction

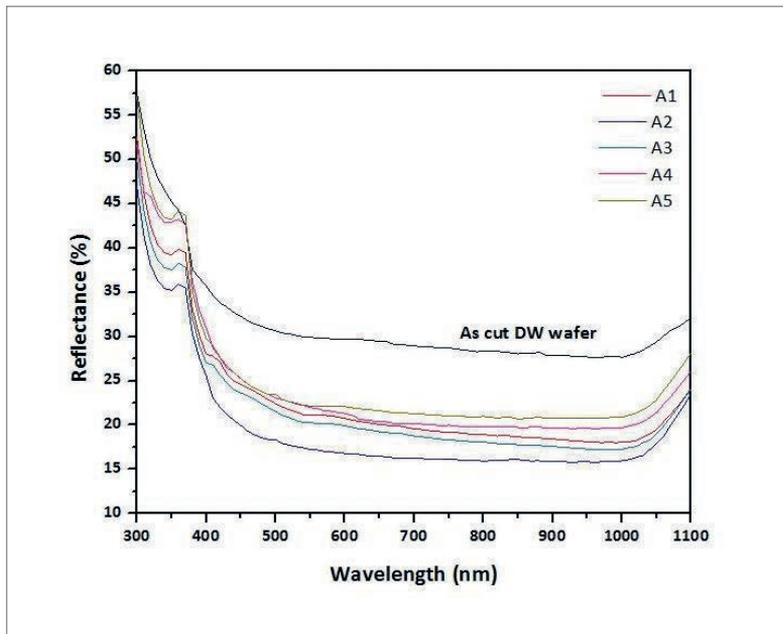
Crystalline silicon PV with slurry wire (SW)-cut wafers as the initial raw material has dominated the PV industry since its early beginnings [1,2]. Although SW slicing with a slurry of SiC abrasives is the most widely used in the silicon wafer slicing industry, it produces wafers with high surface mechanical damage and high associated kerf losses [3]. In addition to the wafer production concerns, SW slicing has significant environmental waste because of the inordinate consumption of wire for sawing [4,5].

In order to overcome the aforementioned issues, an alternate sawing method, namely diamond wire (DW) cutting technology, has been introduced in the slicing industry [6,7]. Many research groups have reported [8–13] that DW cutting technology is recognized for its higher productivity and lighter wearing of the wire. However, DW cutting technology has not completely eliminated SW slicing technology, because the DW-cut wafers exhibit a non-uniform surface roughness compared with the SW-cut wafers.

In the conventional silicon solar cell process, saw damage etching, surface texturing and surface cleaning are the crucial steps in fabricating high-efficiency cells in mass production at low cost. Reducing the surface reflectance of the silicon wafers by surface texturing is a significant step in enhancing the efficiency of the solar cells. In the solar cell manufacturing industry, various wafer etching processes for etching SW-cut wafers have become established, such as isotropic and anisotropic etching. Although DW cutting technology has been used initially for slicing monocrystalline silicon wafers [10], it has not been widely adopted because the alkaline texture process is not capable of producing the expected texture surface. Whereas the alkaline texture process on SW-cut monocrystalline silicon wafers leaves deeper damage, in DW-cut wafers the damage is less but concealed by amorphous silicon, which forms because of the high-speed sawing nature of DW technology. In consequence, the DW wafers are left with high saw marks and a badly damaged wafer surface, which results in higher reflection and thus lower performance. Hence an additional, simple precleaning process using tetramethyl ammonium hydroxide (TMAH) has been included [14] along with the regular texture process, so that the high saw marks with amorphous silicon can be removed, resulting in the formation of a random pyramid structure. The texture process has been developed for DW-cut *monocrystalline* silicon wafers; however, it is important to check that this slicing technology is suitable for *multicrystalline* silicon wafers, now that these wafers are gaining a significant share in silicon solar cell production.

As might be expected, the light reflectance is high in the case of the conventional acidic texturing process with DW-cut wafers. In the literature certain processes have been reported to reduce the light reflection and thus enhance the electrical performance, specifically processes such as reactive ion etching [15], metal-assisted texturing [16], the addition of sulphuric acid [11] in the acidic texturing mixture (hydrofluoric acid and nitric acid), vapour blast etching [12] or a texture additive solution [17]. Among these processes, the addition of  $H_2SO_4$  in a HF/HNO<sub>3</sub> mixture [11] and adding a texture additive solution in a HF/HNO<sub>3</sub> mixture are the simplest and least expensive processes. The studies

**“DW cutting technology is recognized for its higher productivity and lighter wearing of the wire, but the DW-cut wafers exhibit a non-uniform surface roughness.”**



**Figure 1. Reflectance of an as-cut DW wafer and of wafers textured without (A1) and with (A2–A5) texture additive A.**

on the addition of  $H_2SO_4$  in a  $HF/HNO_3$  mixture have demonstrated a reasonable reduction in light reflection [11], and have also shown that there is still more scope for improvement.

In the present study, an optimization of saw damage removal and texturization for DW-cut wafers by using a texture additive has been carried out. A commercially available texture additive solution, referred to as 'A' (the actual name of the texture additive solution is not disclosed here to maintain confidentiality), was used for optimizing the texturization of DW-cut wafers. In order to achieve the best performance, different etch depths were tried, but keeping the wafer source the same. Mean reflectance and surface morphology investigations were also performed. Different etch depth wafers were processed by using a conventional silicon solar cell process to create the solar cells. *I–V* studies were carried out and the results interpreted with regard to mean reflectance and surface morphology.

### Experiment

Boron-doped DW-cut multicrystalline silicon wafers of size  $156.75\text{mm} \times 156.75\text{mm}$ , with a thickness of  $200 \pm 20\mu\text{m}$  and a bulk resistivity of  $0.5\text{--}3.0\Omega\text{cm}$ , were taken as the starting material. Silicon solar cells were fabricated by employing conventional screen-printing technology and the following process flow (in brief):

- Saw damage removal and texturization
- P diffusion
- Wet edge isolation and phosphosilicate glass (PSG) removal

**Table 1. Reflectance and etch depth of as-cut and textured wafers, without and with additive A.**

Sample	Raw wafer	Textured w/o additive	Textured with additive A			
		A1	A2	A3	A4	A5
Reflectance [%]	42	24.18	19.54	22.09	21.99	24.73
Etch depth [ $\mu\text{m}$ ]	N/A	5.5	1.8	2.5	3.0	4.5

- Anti-reflection coating (ARC)
- Back-contact and back-surface field (BSF) printing and drying
- Front-contact printing and drying
- Co-firing

Reflectance studies on bare DW-cut wafers, and on wafers processed with and without texture additive A for different etch depths, were carried out in the wavelength range 300–1100nm. The texture uniformity and surface morphology of the DW wafers were examined using scanning electron microscopy (SEM), and the results compared with SW wafers. (The texture additive details, corresponding labelling of samples, reflectance and etch depth of these samples are shown later, in Table 1.) These DW-cut wafers were then processed to create solar cells. The *I–V* studies of the finished solar cells were performed under AM 1.5G simulated solar radiation at  $25^\circ\text{C}$  by using an AAA solar simulator.

## Results and discussion

### Reflectance studies

Fig. 1 shows the reflectance of as-cut DW wafers and of wafers textured without (A1) and with (A2–A5) the texture additive A. For efficient solar cells, the reflectance should be minimal. From Fig. 1 it is seen that the mean reflectance of an as-cut DW Si wafer between 300nm and 1100nm wavelengths is 42.0%, while the etch depth and the mean reflectance of DW-cut wafers processed without texture additive A are  $5.5\mu\text{m}$  and 24.18% respectively. The surface of the textured DW-cut wafers is shiny with sawing grooves, whereas SW-cut wafers have a matte finish.

In order to optimize the texturization process recipe with the texture additive A for DW-cut wafers, it was decided to combine the additive as per the supplier's recommendation with existing  $HF/HNO_3$  in the ratio 1.0:1.5. By varying either the process temperature or the transport speed, experiments for different etch depths were conducted and labelled A2–A5. The texturing process of the texture additive A with  $HF/HNO_3$  leads to reduced mean reflectance. The as-cut DW wafer and the wafer textured without texture additive A have a mean reflectance of 42.0% and 24.18% respectively, whereas after etching to a depth of  $1.8\mu\text{m}$  with the additive, the mean reflectance drops to 19.54% (A2). However, in order to determine an optimized etch depth with a suitable mean reflectance, it was decided to perform the experiments with different etch depths. The mean reflectances for the different etch depth experiments are listed in Table 1.

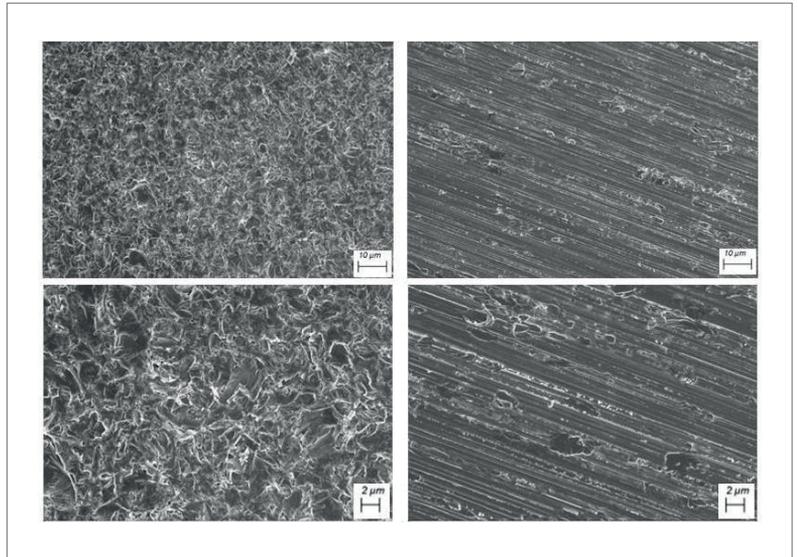
After incorporating the texture additive, the etch depth and mean reflectance decrease dramatically (for the same temperature and transport speed); for the etch depth of  $1.8\mu\text{m}$ , the mean reflectance observed is 19.54%. Although the mean reflectance is lower, the surface was not uniformly etched because of the preferential etching over the DW wafer surface. It was therefore decided to study the reflectance at different etch depths. With increasing etch depth, it was found that the reflectance increases: when  $2.5\mu\text{m}$  of the Si is removed, the mean reflectance is higher (22.09%) than for  $1.8\mu\text{m}$  (19.54%), whereas the mean reflectance for wafers etched  $3.0\mu\text{m}$  (21.99%) is almost the same as for  $2.5\mu\text{m}$  (22.09%). Further etching was also carried out to study the changes in reflectance. It was observed that for a  $4.5\mu\text{m}$  etch depth, the mean reflectance was 24.73%. From Table 1 it is evident that an etch depth of  $1.8\mu\text{m}$  yields the lowest reflectance; however, before taking  $1.8\mu\text{m}$  to be an optimized etch depth, it is essential to consider the surface morphology and interpret this with respect to etch depth.

**Surface morphology**

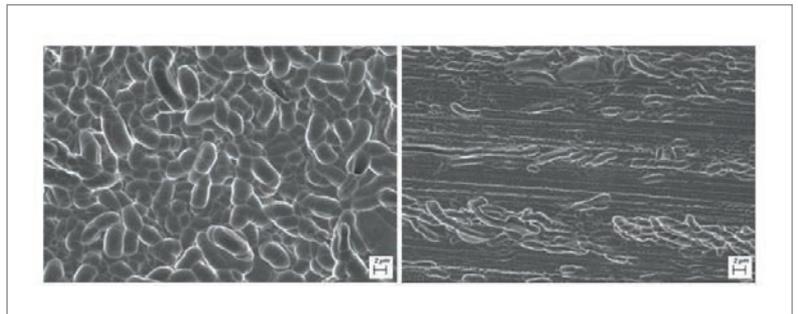
SEM images of the surface morphology of as-cut SW and DW wafers are shown in Fig. 2. The image for the as-cut DW wafer reveals that the wafers contain saw marks, which are due to the scoring by the diamond particles over the silicon surface. From Fig. 2 it can be seen that the regions of surface damage are around  $4\mu\text{m}$  in size. Many areas where the silicon has chipped off are also observed, along with the saw marks; this may be caused by the stress of diamond granules on the wire against the multicrystalline silicon surface. The surface of the as-cut SW wafers appears rougher than that of the as-cut DW wafers, and the sawing direction is not noticeable. The initial step in the silicon solar cell process is etching, in which the removal of saw marks and the texturization to reduce the reflection are done simultaneously.

When the surface morphologies are compared, the same kind of etching process for both as-cut DW and SW wafers will clearly never be adequate in removing the saw damage and in texturizing. In general, the surface of the SW wafers lacks amorphous silicon, whereas the surface of the DW wafers is covered with it; this important difference arises because of the nature of the sawing mechanisms. The amorphous silicon safeguards the surface of the DW wafer from conventional acidic etching. It is therefore important to overcome this concern either by changing the etching chemistry or by varying the etching process time. Alternatively, the DW sawing mechanism should be modified in such a way that the formation of amorphous silicon is avoided.

Conventional  $\text{HF}/\text{HNO}_3$  acidic etching has been carried out on both SW- and DW-cut wafers. Fig. 3 depicts the surface morphologies of both the wafers after undergoing saw damage removal and



**Figure 2. Surface morphology (lower and higher magnification) of as-cut SW (left) and DW (right) wafers.**

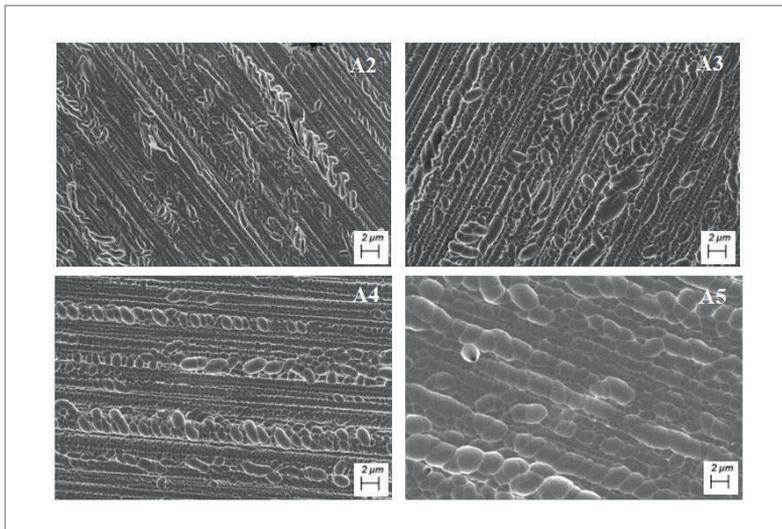


**Figure 3. Surface morphology of textured SW and DW wafers.**

texturization. As discussed earlier, the sawing mechanisms of SW and DW yield different surface structures on as-cut wafers, which result in significant effects on the wafer surface morphologies because of acidic etching.

The mean reflectances observed for SW and DW wafers after texturing are 23.6% and 24.18% respectively. The etch depth of both DW and SW wafers is the same ( $5.5\mu\text{m}$ ) as a result of acidic etching, but the surface looks different. The SEM image of the surface of the textured SW silicon wafers reveals that the etching has been performed homogeneously, with wormlike pits of width  $2\mu\text{m}$  across the wafer. The surface of the textured DW-cut wafers, however, appears to indicate that the texturization is not fully completed. This shows that the same acidic etch mixtures and etch parameters used for etching SW wafers are not suited to etching DW-cut wafers. From Fig. 3 it can be seen that the acidic texturing leads to elliptical pits distributed randomly across the wafer, with grooving also occurring. Although the saw marks are smaller than in the case of the as-cut wafer, the acidic texturing did not remove the saw mark grooves completely. A

**“The same kind of etching process for both as-cut DW and SW wafers will clearly never be adequate in removing the saw damage and in texturizing.”**



**Figure 4. Surface morphologies of textured DW wafers with texture additive A, for different etch depths (A2–A4).**

systematic investigation was carried out to eliminate the saw marks by effective surface texturing on DW wafers with the use of a commercially available texture additive.

Fig. 4 shows the surface morphology of DW-cut wafers textured with texture additive A for different etch depths. If the surface of the DW wafers textured with and without additive are compared, it is seen very clearly that the wafers processed without the texture additive in an acidic etching process yield an inhomogeneous silicon surface; this results from the presence of amorphous silicon on the wafer surface, and thus from the non-uniform reactivity of the acidic etchant over the DW wafer surface.

In contrast, the surface of the textured wafers processed with the texture additive are enriched with micro pits, for all the different etch depths. It is observed that the uniformity and size of the pits increases with increasing etch depth. Furthermore, no grooves are found on the wafers processed with etch depths greater than  $1.8\mu\text{m}$ , from which it can be inferred that the saw marks are completely removed. Since the wafer surfaces possess a uniform texture at an etch depth of  $4.0\mu\text{m}$ , it was decided to halt the etching experiments, and move on to processing solar cells from wafers with the various etch depths.

### Solar cell performance

Table 2 shows the electrical characteristics of solar cells with different etch depths. Solar cells of area  $245.71\text{cm}^2$  were measured with a light irradiation of  $1,000\text{W}/\text{m}^2$ . From the electrical characteristics, it is

**Table 2. Electrical parameters of solar cells for different etch depths.**

Parameter	Textured w/o additive	Textured with additive A			
	A1	A2	A3	A4	A5
Efficiency [%]	18.17	18.13	18.40	18.36	18.29
Power $P_{\text{mpp}}$ [Wp]	4.46	4.46	4.52	4.51	4.49
Short-circuit current $I_{\text{sc}}$ [A]	8.82	8.86	8.90	8.89	8.86
Open-circuit voltage $V_{\text{oc}}$ [mV]	629.0	626.9	631.4	630.9	630.8
Fill factor $FF$ [%]	80.44	80.19	80.37	80.38	80.41

observed that cells processed with texture additive demonstrate better performance than with just the conventional acidic process.

Wafers with an etch depth of  $2.5\mu\text{m}$  show better performance than that at other etch depths. Although the mean reflectance is slightly higher than that of the  $1.8\mu\text{m}$  etch depth, the morphology of wafers etched to  $2.5\mu\text{m}$  does not exhibit any saw marks. Hence, it is clear that not only do the optical properties of the front surface have an impact on the electrical parameters, but also the surface texturization plays an important role in electrical performance. Similarly, SEM studies revealed that  $4.5\mu\text{m}$ -etched wafers have a homogeneous textured surface; however, the mean reflectance is higher than that of the  $2.5\mu\text{m}$ -etched wafers.

A comparison of the electrical parameters for different etch depth wafers reveals that there is not much difference in  $I_{\text{sc}}$  and  $FF$ , but the  $V_{\text{oc}}$  is higher in  $2.5\mu\text{m}$ -etched wafers; this may be due to the lower surface and auger recombination. It is important to note that the lower mean reflectance (optical loss) and lower recombination (electrical loss) resulted in the superior performance for  $2.5\mu\text{m}$ -etched DW-cut wafers.

### Conclusions

Current studies on DW-cut wafers, reported in this paper, have revealed that the conventional acidic texturing process is not effective, because of the non-homogeneous texturing and thus the DW saw marks not being completely removed. In this paper, a systematic approach to optimizing the texturing process with the use of a texture additive has been taken, by etching DW wafers at different etch depths. Optical and morphological studies were carried out to interpret the reflectance and surface nature for different etch depths. For investigating all etch depths, multicrystalline silicon solar cells of size  $156.75\text{mm} \times 156.75\text{mm}$  were fabricated by using a conventional silicon solar cell process. The wafers processed with a texture additive and an etch depth of  $2.5\mu\text{m}$  resulted in cells of efficiency 18.40% in an industrial production line. The optical and morphological results confirmed that the enhanced performance is due to the lower mean reflectance (optical loss) and the lower recombination (electrical loss).

### Acknowledgements

The authors thank the management and the cell fab team at RenewSys India Pvt. Ltd. for their support.

**References**

[1] Möller, H.J. et al. 2004, "Basic mechanisms and models of multi-wire sawing", *Adv. Eng. Mater.*, Vol. 6, pp. 501–513.

[2] Möller, H.J. et al. 2005, "Multicrystalline silicon for solar cells", *Thin Solid Films*, Vol. 487, pp. 179–187.

[3] Chen, W. et al. 2014, "On the nature and removal of saw marks on diamond wire sawn multicrystalline silicon wafers", *Mater. Sci. Semicon. Proc.*, Vol. 27, pp. 220–227.

[4] Watanabe, N. et al. 2010, "Characterization of polycrystalline silicon wafers for solar cells sliced with novel fixed-abrasive wire", *Prog. Photovolt: Res. Appl.*, Vol. 18, pp. 485–490.

[5] Meinel, B., Koschwitz, T. & Acker, J. 2012, "Textural development of SiC and diamond wire sawed sc-silicon wafer", *Energy Procedia*, Vol. 27, pp. 330–336.

[6] Möller, H.J. et al. 2011, "Growth optimization of multicrystalline silicon", *Energy Procedia*, Vol. 3, pp. 2–12.

[7] Wu, C. et al. 2001, "Near unity below bandgap absorption by microstructured silicon", *Appl. Phys. Lett.*, Vol. 78, pp. 1850.

[8] Zhuang, Y.F. et al. 2016, "Versatile strategies for improving the performance of diamond wire sawn mc-Si solar cells", *Sol. Energy Mater. Sol. Cells*, Vol. 153, pp. 18–24.

[9] Cao, F. et al. 2015, "Next generation multi crystalline silicon solar cells: Diamond wire sawing, nano texture and high efficiency", *Sol. Energy Mater. Sol. Cells*, Vol. 141, pp. 132–138.

[10] Chen, K. et al. 2015, "Novel texturing process for diamond-wire-sawn single-crystalline silicon solar cell", *Sol. Energy Mater. Sol. Cells*, Vol. 133, pp. 148–155.

[11] Lippold, M. et al. 2014, "Texturing of SiC slurry and diamond wire sawn silicon wafers by HF-HNO<sub>3</sub>-H<sub>2</sub>SO<sub>4</sub> mixtures", *Sol. Energy Mater. Sol. Cells*, Vol. 127, pp. 104–110.

[12] Chen, W. et al. 2014, "On the nature and removal of saw marks on diamond wire sawn multicrystalline silicon wafers", *Mater. Sci. Semicon. Proc.*, Vol. 27, pp. 220–227.

[13] Bidiville, A. et al. 2009, "Diamond wire sawn silicon wafers – From the lab to the cell production", *Proc. 24th EU PVSEC*, Hamburg, Germany.

[14] Papet, P. et al. 2006, "Pyramidal texturing of silicon solar cell with TMAH chemical anisotropic etching", *Sol. Energy Mater. Sol. Cells*, Vol. 90, pp. 2319–2328.

[15] Yoo, J., Yu, G. & Yi, J. 2011, "Large area multicrystalline silicon solar cell fabrication using reactive ion etching (RIE)", *Sol. Energy Mater. Sol. Cells*, Vol. 95, pp. 2–6.

[16] Kumagai, A. 2015, "Texturization using metal catalyst wet chemical etching for multicrystalline diamond wire sawn wafer", *Sol. Energy Mater. Sol. Cells*, Vol. 133, pp. 216–222.

[17] Sankarasubramanian, S. et al. 2015, "Impact of surface texturization on overall performance of mono-crystalline silicon solar cells, *ECS Trans.*, Vol. 66, No. 6, pp. 9–17.

**“The lower mean reflectance (optical loss) and lower recombination (electrical loss) resulted in the superior performance for 2.5µm-etched DW-cut wafers.”**

**About the Authors**



S. Saravanan received his Ph.D. in physics from the Cochin University of Science and Technology, India, in 2005, after which he worked as a postdoctoral fellow at the ADFA at UNSW, Canberra, and at the IISc, Bangalore. Since 2007 he has been working on silicon photovoltaics, initially for TATA BP Solar India Ltd and then for NCPRE, IIT Bombay. In 2016 he joined RenewSys India Pvt. Ltd. as an R&D manager, working on high-efficiency silicon solar cells.



Ch.S.R. Suresh is a deputy manager at RenewSys India Pvt Ltd, Hyderabad, where he is responsible for cell line operations. He specializes in screen-printing technologies for solar cell applications. Prior to joining RenewSys, he gained experience in GaAs MMIC and solar PV.



V.V. Subraveti works as an assistant general manager at RenewSys India Pvt Ltd, Hyderabad, and is responsible for solar PV cell manufacturing operations. Before joining RenewSys, he gained experience in GaAs MMIC technologies and solar PV.



K.C. Kumar is vice president of RenewSys India Pvt Ltd, Hyderabad, where he focuses on cell and module technologies, materials, manufacturing operations and strategic planning. Prior to joining RenewSys, he worked on various semiconductor device technologies, including Si CMOS, GaAs MMIC and Si solar PV.



U.K. Jayaram is executive director of RenewSys India Pvt Ltd, where he oversees activities in solar PV cell and module technologies, materials, components and manufacturing processes.

**Enquiries**

S. Saravanan  
 RenewSys India Pvt Ltd, Hyderabad – 501 359  
 Telangana, India  
 Tel: +91 9611222788  
 Email: saravanan.somasundaram@renewsysindia.com  
 Website: www.renewsysworld.com